Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently Amended) A dynamic random access memory device, comprising:

an address bus interface;

an address bus termination circuit that can be enabled or disabled; ~~and~~

an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level;

a data bus interface;

a data bus termination circuit that can be enabled or disabled; and .

a data bus termination control signal input, wherein the data bus termination control signal input is operable to enable the data bus termination circuit when the data bus termination control signal input is tied to a first voltage level, and wherein the data bus termination control signal input is operable to disable the data bus termination circuit when the data bus termination control signal input is tied to a second voltage level.

2. (Original) The memory device of claim 1, the address bus termination circuit to be enabled if an asserted address bus termination control signal is received at the address bus termination control signal input.

3. (Original) The memory device of claim 2, the address bus termination circuit to be disabled if the address bus termination control signal is not asserted.

4. (Original) The memory device of claim 3, wherein the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level.

5. (Original) The memory device of claim 3, wherein the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

Claims 6-7 (Cancelled)

8. (Currently Amended) A memory module, comprising:

a plurality of dynamic random access memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of dynamic random access memory devices including

an address bus interface,

an address bus termination circuit that can be enabled or disabled, and

an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level,

a data bus interface;

a data bus termination circuit that can be enabled or disabled; and .

a data bus termination control signal input, wherein the data bus termination control signal input is operable to enable the data bus termination circuit when the data bus termination control signal input is tied to a first voltage level, and wherein the data bus termination control signal input is operable to disable the data bus termination circuit when the data bus termination control signal input is tied to a second voltage level.

9. (Original) The memory module of claim 8, wherein for each of the plurality of memory devices the address bus termination circuit is enabled if an asserted address bus termination control signal is received at the address bus termination control signal input.

10. (Original) The memory module of claim 9, wherein for each of the plurality of memory devices the address bus termination circuit is disabled if the address bus termination control signal is not asserted.

11. (Original) The memory module of claim 10, wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level.

12. (Original) The memory module of claim 11, wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to ground and the last memory device in the daisy chain configuration has its address bus termination control signal tied to a positive voltage.

13. (Original) The memory module of claim 10, wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

14. (Original) The memory module of claim 13, wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to a positive voltage and the last memory device in the daisy chain configuration has its address bus termination control signal tied to ground.

Claims 15-20 (Cancelled)